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TEKSCOPE

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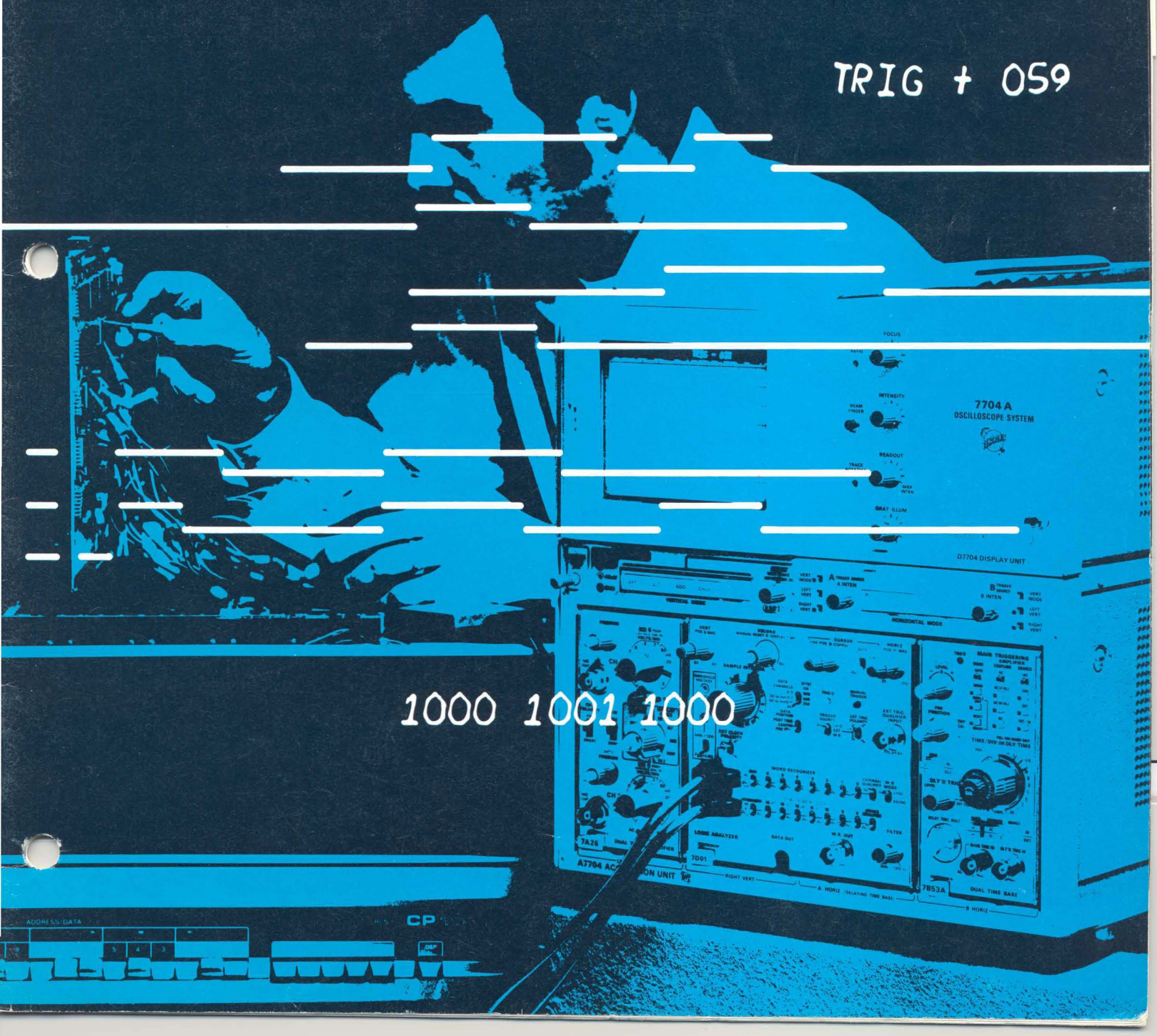

TEKSCOPE

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Servicescope, a regular feature, does not appear in this issue because of space considerations. It will resume in the next issue.

Cover: Some of the unique features of the 7D01/7000 Series logic analyzer system are presented in this artistic treatment. The digital readout above the traces shows the number of clock pulses occurring between the trigger and cursor positions. The readout below the traces is the binary word present at the cursor position. (The trigger and cursor position are not shown in this display.)

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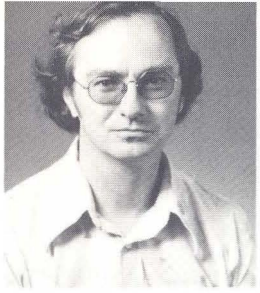


Keith Taylor

A 16-channel logic analyzer for the 7000 Series

More than just an oscilloscope. This is the phrase often used to describe the 7000 Series. And for good reason. Plug-in versatility transforms 7000 Series Oscilloscopes into counters, digital multimeters, spectrum analyzers, time-domain reflectometers, curve tracers, rapid-scan spectrometers, etc. Now, with the introduction of the 7D01 plug-in, 7000 Series Oscilloscopes become state-of-the-art logic analyzers.

The 7D01 is a 16-channel, logic timing analyzer that presents data in the familiar oscilloscope-type, time-related diagram pictured in figure 1. But, as you can see, there's much more that meets the eye in figure 1 than just the usual multi-trace, logic timing diagram. Several features have been added to aid you in analyzing the displayed data.

Note the two vertical rows of bright dots. The row at the left indicates the triggering point. In this instance, we have selected the post-trigger position, which means that 90% of the data displayed occurs after the trigger. Pre-trigger and center-trigger positions are available at the flip of a switch, to give you a wide range of data to view.

The second row of bright dots in the display provides a reference point for making time comparisons between displayed channels. This row of dots can be positioned anywhere on the horizontal axis by means of the cursor

controls. The fine control moves the dots one bit at a time, and the coarse control in 16-bit increments. The readout at the top of the screen shows the number of bits occurring between the trigger and the cursor. In the asynchronous mode, this number multiplied by the sample interval equals the time difference between the trigger and the cursor position. When using an external clock, the readout shows the number of clock pulses occurring between these two points. The cursor is especially convenient for locating a particular bit or point in time relative to the trigger.

There has been much discussion as to whether the logic state or the logic timing display is the most useful in performing logic analysis. Each has advantages for specific applications. The 7D01 resolves this issue for many applications by providing both types of display.

You will note that the readout at the bottom of the screen in figure 1 is in the format usually displayed by logic state analyzers. The binary word displayed corresponds to the logic word present at the cursor position. This unique feature makes the 7D01 useful for many software and firmware applications. It is often a convenience also in hardware applications.

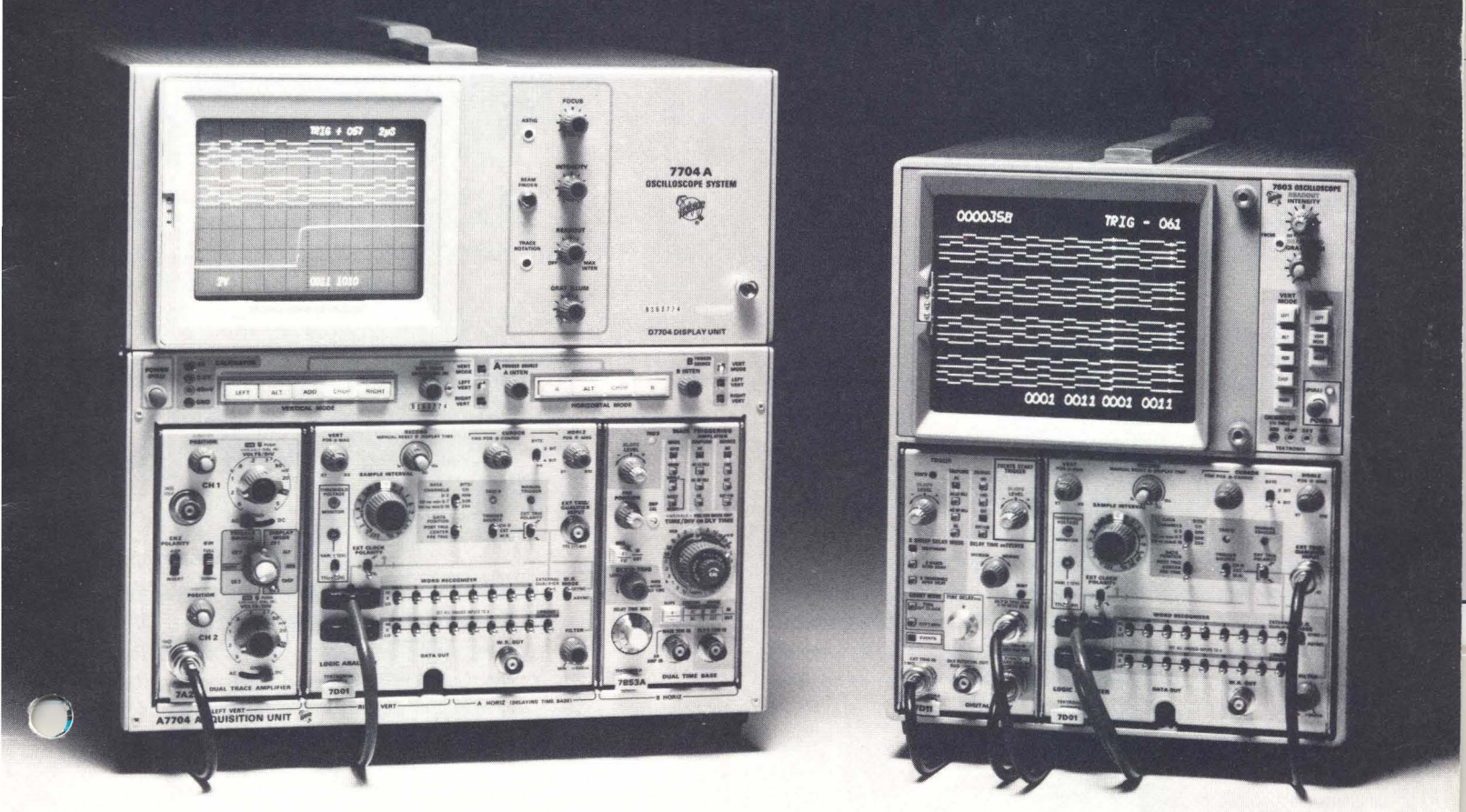
A versatile trigger

Trigger versatility is one of the most important characteristics of a logic analyzer. We have already discussed the ability to view data preceding the trigger, following the trigger, or both preceding and following the trigger. Now, let's consider the sources of trigger.

A choice of three sources is provided by a front-panel switch: channel 0 of the probe input, external via BNC input, or from the built-in, 16-bit Word Recognizer. A fourth choice is manual triggering by front-panel pushbutton.

The 16 data-input channels also serve as inputs for the Word Recognizer. Front-panel switches allow you to select any pattern of up to 16 parallel bits as the trigger word.

Two additional inputs, the Probe Qualifier and the External Qualifier, provide still further selection of the triggering point, giving us, in essence, an 18-bit Word Recognizer. The External Qualifier may be the output from another Word Recognizer, a time delay or digital delay generator, or another signal from the system under test. The signal should be TTL level and have a minimum duration of 15 ns.



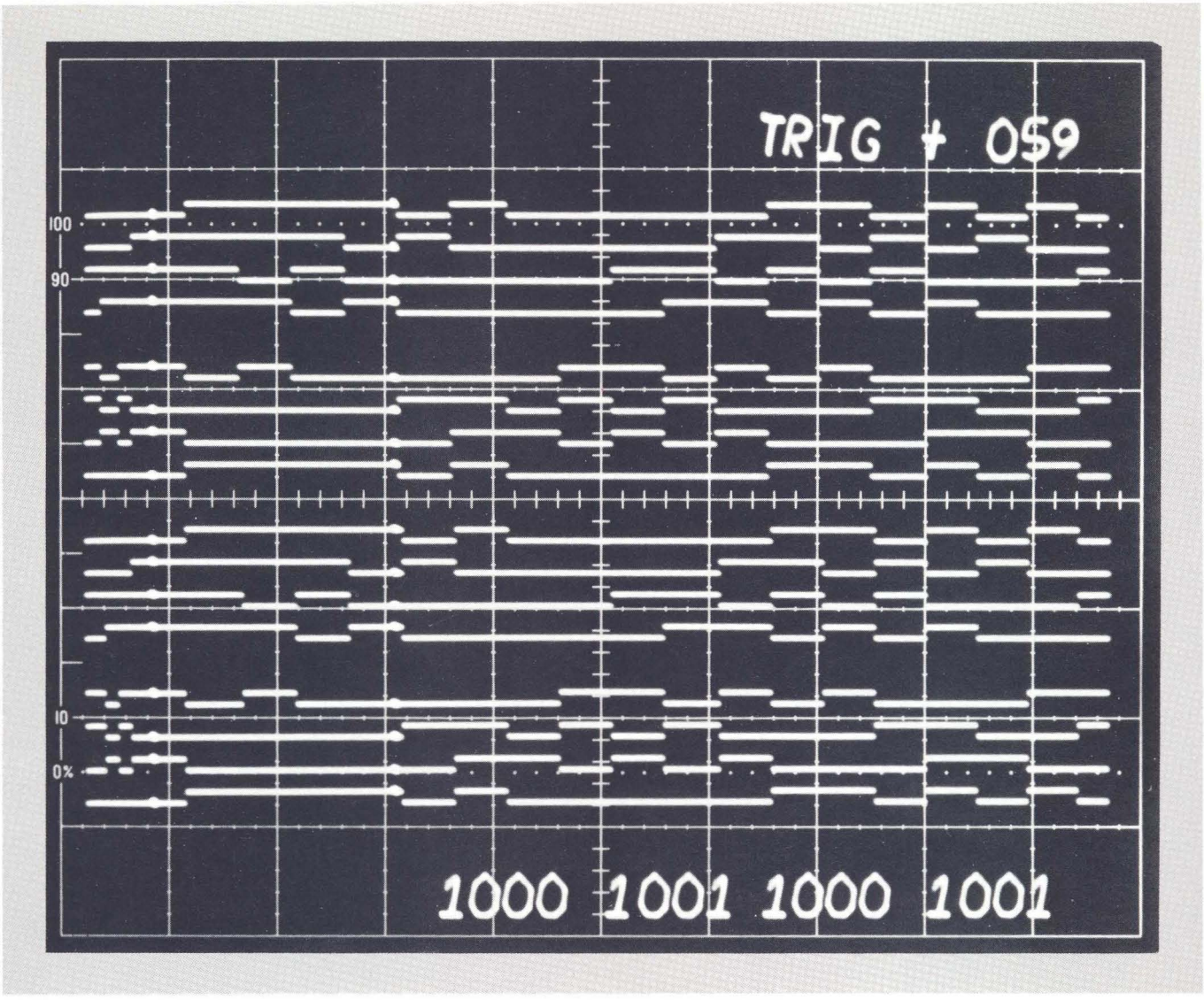


Fig. 1. A wealth of information is available from the display generated by the 7D01. The intensified dots at left show the trigger point. The dots about two divisions to the right are a movable cursor. The number of clock pulses occurring between the two bright dots is displayed at the top of the screen. The 16-bit binary word at the cursor position is displayed at the bottom of the screen. Right to left corresponds with top to bottom.

There are two paths through the Word Recognizer, synchronous and asynchronous, selectable by a front-panel switch. In the asynchronous mode, a variable filter is inserted in the trigger path that prevents glitches and other anomalies from causing false triggering. Word recognition of bit combinations of shorter duration than the filter setting is inhibited. Maximum filter width is at least 300 ns.

The trigger point indicated on the display is most accurate when operating the Word Recognizer in the asynchronous mode with the filter set at minimum, or when using an external sampling interval. The trigger position indication is less accurate when triggering from channel 0, or when the asynchronous filter is advanced clockwise.

The built-in Word Recognizer operates independent of the rest of the logic analyzer. When all of the conditions required for word recognition are met, the data acquisition circuits are enabled and a HI signal is supplied to a front-panel connector, for triggering an oscilloscope or other associated equipment. A Word Recognizer output occurs each time the conditions are met, whether the logic analyzer is operating in the store or display mode.

For applications where it is desirable to page through a long sequence of events, a companion plug-in, the 7D10, provides digital delay by up to 10^7 events. The delayed trigger output of the 7D10 serves as an external qualifier or trigger for the 7D01. The 7D10 counts events at rates up to 50 MHz.

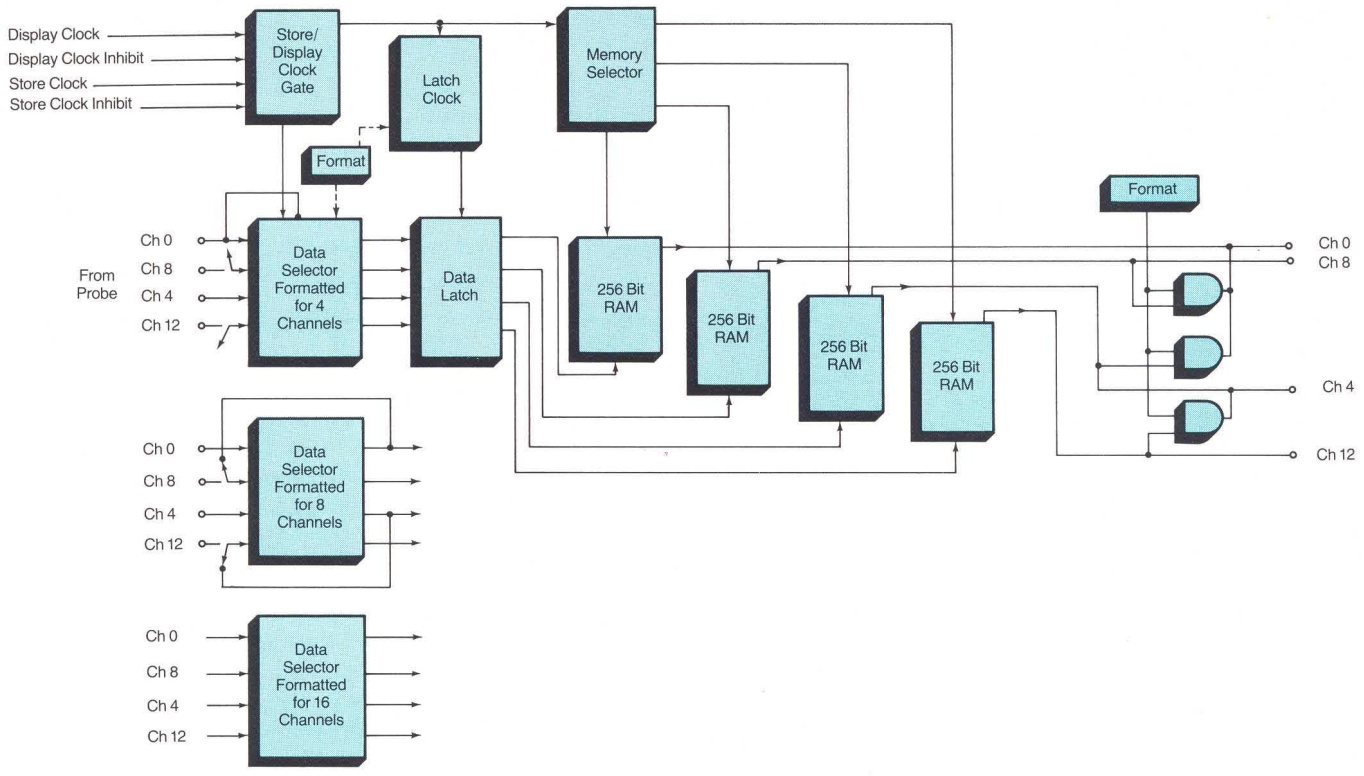


Fig. 2. The 4-k memory in the 7D01 is formattable. One of four 4 x 256-bit sections is shown. It can store 1024 bits from one channel, 512 from two, or 256 from four channels. In 4-channel operation the Data Selector functions as a 4-bit shift register, in 8- and 16-channel operation as 4-bit latches.

Data inputs

Up to 16 channels of parallel data can be acquired simultaneously by the 7D01. Minimum loading (1 MΩ, 5 pF) on the circuit under test is achieved by two active probes with multiple inputs. Probe qualifier and external clock inputs are also provided for in the active probes.

You have a choice of threshold levels for the probe inputs — a preset +1.4 volts for TTL applications, or selection over a range of ± 12 volts by a front-panel variable control.

Data can be clocked into the 7D01 in either a synchronous or asynchronous mode. In asynchronous, the clock may be either internal or external at rates up to 100 MHz depending upon the number of channels in use. To match the resolution of the measurement to your specific application, sample intervals derived from the internal clock may be selected over the range of 5 ms to 10 ns, in a 1-2-5 sequence.

A formattable memory

One of the most useful features of the 7D01 is the formattable memory. Consisting of sixteen 256-bit random access memories (RAMs), the memory can be formatted by a front-panel switch to store four channels with 1024 data bits per channel, eight channels with 512 bits per channel, or sixteen channels with 256 bits per channel.

Let's take a look at how this is accomplished (see figure 2). The 16 data inputs are arranged in groups of four, each group coupled to a corresponding 4 x 256-Bit RAM. In the 4-channel mode of operation, the Data Selector functions as a 4-bit shift register, acquiring four bits of data input from channel 0. The Data Latch transfers the data from the outputs of the Data Selector to the inputs of the four, 256-Bit RAMs. Through a three-gate arrangement controlled by the DATA CHANNELS switch, the outputs of the RAMs can be added to give us a single 1024-bit memory, two 512-bit memories, or four 256-bit memories. The function of the Data Selector is also controlled by the DATA CHANNELS switch to pass four bits of data from one channel, two bits from each of two channels, or one bit from each of four channels, to the Data Latch.

Data acquisition and display

Figure 4 is a simplified block diagram of the 7D01. Let's refer to it and go through a cycle of acquiring and displaying data. A good point to start is when reset occurs.

When display time ends, a reset signal is generated by the reset circuitry. This resets the trigger flip-flop, trigger and address counters, and the store/display flip-flop, switching the memory from the display mode to the store mode. Data, which is clocked into the Data Latch at the high-frequency clock rate, is transferred to the

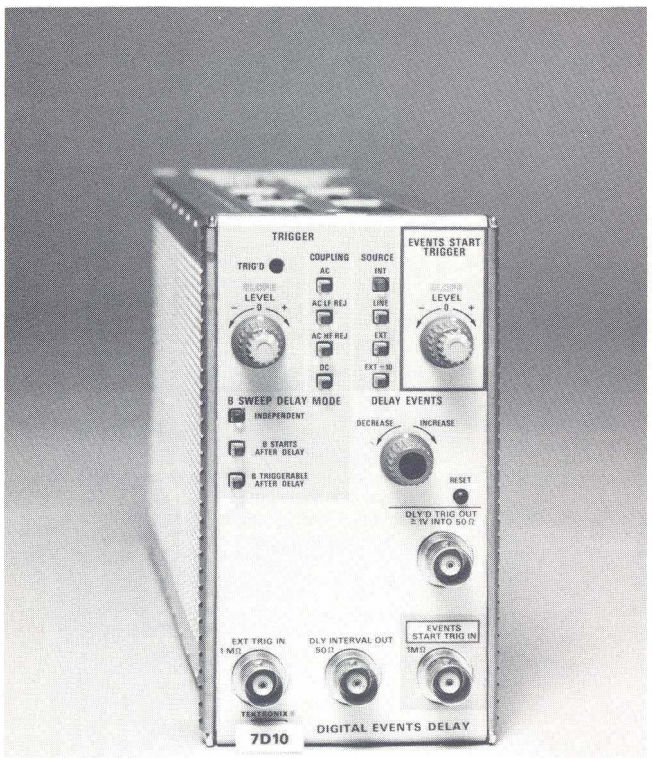


Fig. 3. The 7D10 Digital Delay plug-in is an ideal companion for the 7D01. It will count up to 10^7 arbitrary trigger events, periodic or aperiodic, and deliver an output after the preselected count has been reached.

memory at the memory low-frequency clock rate, starting with the end of reset. The high-frequency clock rate is determined by the SAMPLE INTERVAL switch setting, and is divided by 1, 2, or 4 times to establish the low-frequency clock. Data is clocked into the memory until a trigger occurs, and for a period following the trigger as determined by the DATA POSITION switch setting. For example, in the CENTER position, half of the memory fills after the trigger occurs.

The input steering and latch circuitry determines how data will be input to the memory. In the 4-channel mode, the data from channel 0 is clocked serially into one 4 x 256 section of the memory, as previously discussed. The data from channels 1, 2, and 3 are clocked into their respective memories simultaneously, in a similar manner.

Occurrence of the trigger, switches the trigger flip-flop, gating on the trigger low-frequency clock. The low-frequency clock is the store clock (high-frequency clock) divided by 1, 2, or 4 times, depending upon the setting of the DATA CHANNELS switch. A separate 1-, 2-, or 4-times divider is used for the trigger low-frequency clock because of phasing considerations related to the memory low-frequency clock.

The trigger counter counts 16, 128, or 240 counts (depending upon trigger position selected) and then generates the first flag. During this flag, the memory clock is summed with a gate derived from the trigger clock, to generate a gate that switches the Store/Display Flip-Flop to the display mode. Transition from store to display is thus made in phase with the memory low-frequency clock.

The display clock, which runs at 2 μs, now becomes the high-frequency clock. It, in turn, is divided by 1, 2, or 4 to become the memory and trigger low-frequency clocks. During display time, the outputs of the sixteen, 256-Bit RAMs are displayed in serial fashion, as determined by the Output Steering and Multiplexer circuitry.

In the display mode, the trigger counter counts through 256 counts of the display clock (equivalent to one display line) and generates a second flag. This flag resets the sweep, blanks the crt, and selects the next channel to be displayed. This flag also goes to a divide-by-16 counter that sets a flag when sixteen channels have been displayed. When the display time ends, a reset pulse is generated and the store/display cycle starts again.

To further enhance the flexibility of the 7D01, a choice of two display modes — Full Display or First Trigger — can be selected by positioning an internal jumper. In the Full Display mode, the trigger to the Trigger Flip-Flop is inhibited until the Address Counter has completely cycled. This assures that the memory is filled with valid data.

In the First-Trigger mode, it is conceivable that a trigger may occur before the memory is completely filled. If this occurs, the display is blanked during the time that invalid data would be presented.

Data outputs

Data from the memory is available in both parallel and serial format from an internal 25-pin connector. Also available are the display/store, flag, frame, trigger intensify, and master reset outputs.

Two inputs are made via the connector: record enable and external display clock input. An external display clock is required if the data are to be output to computer for further analysis.

Summary

The 7D01 is designed to offer high-performance, 16-channel logic analysis to 7000 Series users. Used with conventional oscilloscope plug-ins in a four-hole mainframe, you can have both an oscilloscope and a logic analyzer in a single package. The formattable memory offers unparalleled flexibility, and the high-speed data

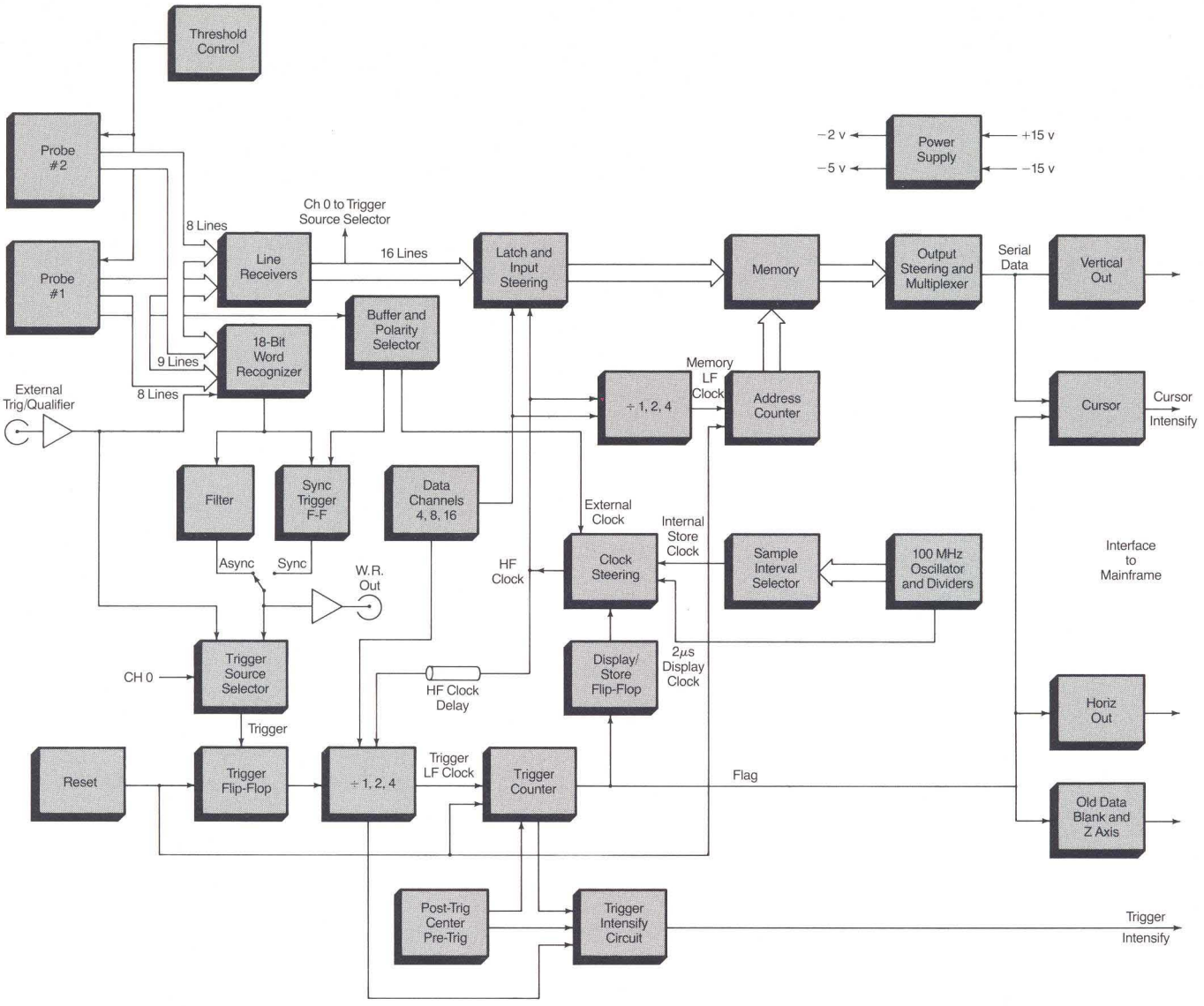


Fig. 4. Simplified block diagram of the 7D01.

acquisition and minimum loading afforded by active probes makes the 7D01 ideal for working with higher speed logic families.

Acknowledgments

Murlan Kaufman as Project Manager provided overall direction for the 7D01. Project Leader was Keith Taylor, with Morris Green and Jeff Bradford doing electrical design, and Ed Wolf mechanical design. Dick Anderson, Group Technician, provided valuable assistance, as did Beverley Kateley and Dona Fricker on prototype assembly and circuit board details. Roy Kaufman, Evaluation Engineer, and Dave McCullough, Marketing Program Supervisor, also made valuable contributions. Our thanks to Wendell Damm for his work on the active probe, and to the many others who contributed to the completion of the project.

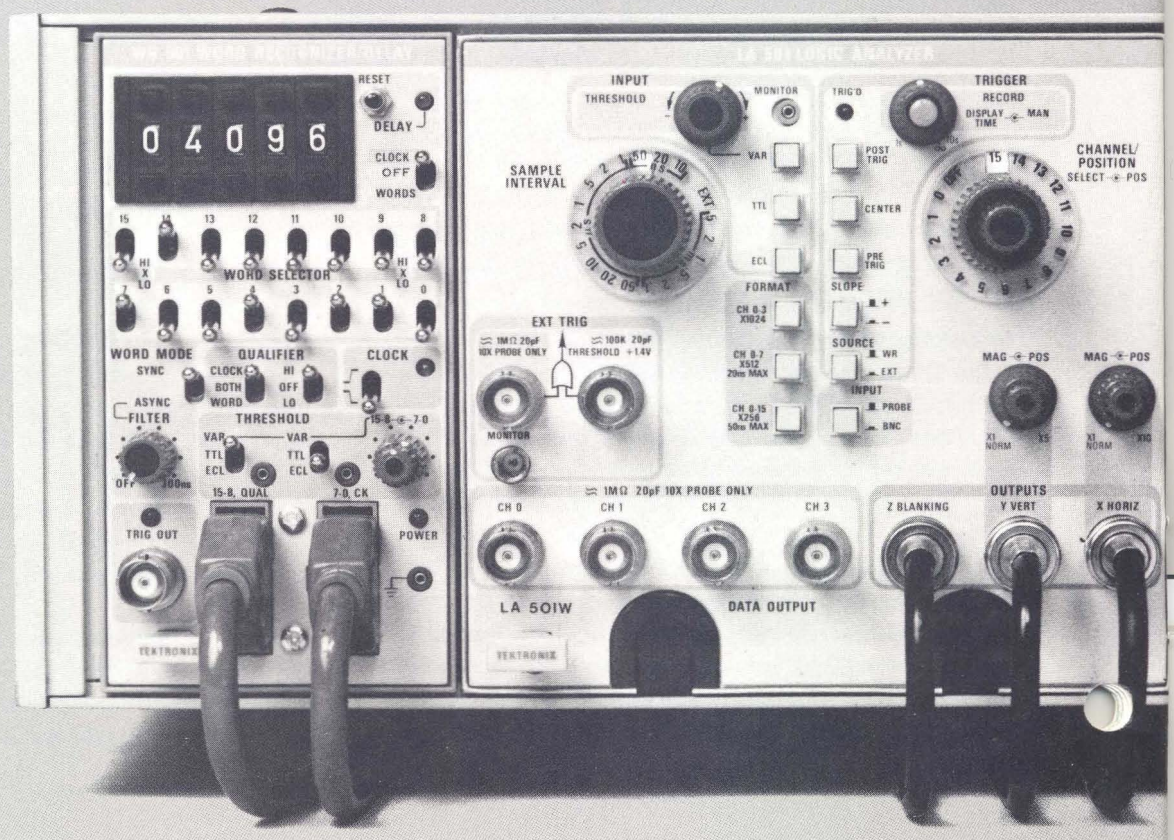
Pete Janowitz

A plug-in word recognizer with digital delay

For sports fans, instant replay quickly became one of the most appreciated improvements in televised sports programming. Engineers have long had the ability to view critical "happenings" in their electronic circuitry, with the aid of oscilloscopes.

Now, with the introduction of logic analyzers, an engineer has not only acquired instant-replay capabilities, he can instantly replay and view sixteen channels simultaneously. It's a companion tool, the word recognizer, that enables him to recapture the action at any point he chooses.

Sometimes the word recognizer is an integral part of the logic analyzer. In other instances, it's a separate entity – like the new TEKTRONIX WR 501 Word Recognizer. Designed primarily to work with the LA 501 Logic Analyzer, it occupies a single plug-in compartment in a TM 500 mainframe. When ordered with the LA 501, the package is called the LA 501W and includes all of the interfacing hardware needed to couple the WR 501 and LA 501 mechanically and electrically.



The WR 501 can also function as a stand-alone word recognizer/digital delay unit for those needing to expand the triggering capabilities of their logic analyzer, oscilloscope or other equipment. For example, WR 501s can be cascaded to obtain greater word width, dual word recognition/delay, or delay "nesting" (delay within a delay).

Using the new P6451 high-impedance (1 MΩ, 5 pF) active probes, the WR 501 can acquire up to sixteen channels of data, plus an external clock and qualifier signal. Maximum flexibility is afforded by using two probes, each with nine inputs. Separate threshold controls for each probe facilitate working with systems using mixed logic families, with preset threshold voltages for TTL and ECL signals selectable by front-panel switches. Variable controls provide a choice of threshold voltage over a range of ± 10 volts.

The Qualifier input can be used to expand the word recognizer to 17 bits, gate the external clock, or do both. In the LA 501W, the external clock can be gated by the Qualifier input, allowing you to selectively clock data into the memory.

Synchronous or asynchronous operation

In some applications it is advantageous for word recognition to be synchronous with the system clock. For others, it is desirable to generate a trigger whenever the word pattern occurs. With the WR 501, the choice is yours at the flip of a switch.

In the synchronous mode, the external clock signal acquired by the probe clocks the Sync Flip-Flop to generate a word recognizer output in step with the system clock.

In the asynchronous mode, a word recognizer output is generated whenever the selected word pattern occurs. A selectable-pulse-width filter with a range of 5 to 300 ns is automatically activated, to reduce the possibility of false triggering due to glitches or data skew.

A built-in digital delay

Another useful feature incorporated in the WR 501 is digital delay. You have a choice of delaying by up to 99,999 clock pulses or words at clock rates up to 50 MHz. Delay by words generates a trigger at the *n*th occurrence of the word so we can see what happens at the end of a program loop, for example. The count is set by convenient push-button thumbwheel switches.

The delay count is started by an output from the word recognizer when word recognition occurs. For those applications where you want to use the delay without the recognizer, you can start the count by using a single bit from one of the data inputs. Just set the appropriate WORD SELECTOR switch. A front-panel push-button lets you reset the delay counter manually at any point in time. Reset is automatic when the selected delay is reached.

The trigger output pulse generated by word recognition, or word recognition plus selected delay, is brought out to a front-panel BNC connector, and also routed to the LA 501 via an internal multi-pin connector. The output pulse is TTL compatible, with duration a function of the operating mode and signal inputs.

Interfacing to the LA 501

Special provisions are made to interface the WR 501 and LA 501 without the need for external connections. The sixteen data inputs, external clock, and word recognizer output are coupled internally through a short cable assembly, to the 25-pin probe-input connector in the LA 501, in place of the P6450 passive probe. The sixteen data inputs to the WR 501 are always present at the interface connector, irrespective of front-panel control settings. This arrangement of the WR 501, interface, and LA 501 make up the LA 501W.

The threshold controls on the WR 501 now control the probe inputs, with the threshold control on the LA 501 affecting only the front-panel external trigger and the BNC probe inputs. Attenuator probes can still be used with the BNC inputs for channels 0 through 3 on the LA 501 by setting the INPUT to BNC. Data channels 4 through 15 will be supplied from the WR 501 inputs. This gives you three individual threshold controls and the ability to view inputs separated some distance. The attenuator probes can handle signals up to ± 500 volts to accommodate many real time situations.

If you have a need for 16-bit word recognition while viewing more than four other data channels, you can remove the interface cable and use the WR 501 as a stand-alone word recognizer. The optional P6450 passive probe can then be used with the LA 501 for data acquisition. The output signal from the WR 501 is coupled externally to the LA 501 external trigger input in this instance.

Technical details

The WR 501 performs two major functions — word recognition and digital delay. The simplified block diagrams in figures 1 and 2 will be useful in understanding how each function is performed, and how they relate.

The sixteen data channels acquired by the WR 501 probes pass through a differential FET pair, with one output going to the word recognizer, and the other output through delay lines to the interface connector. The delay lines provide zero hold time for the LA 501 data inputs.

The Qualifier can gate either the word recognizer or external clock, or both, or can be turned off when not needed. The delay line in the word recognizer signal path provides zero hold time for synchronous operation.

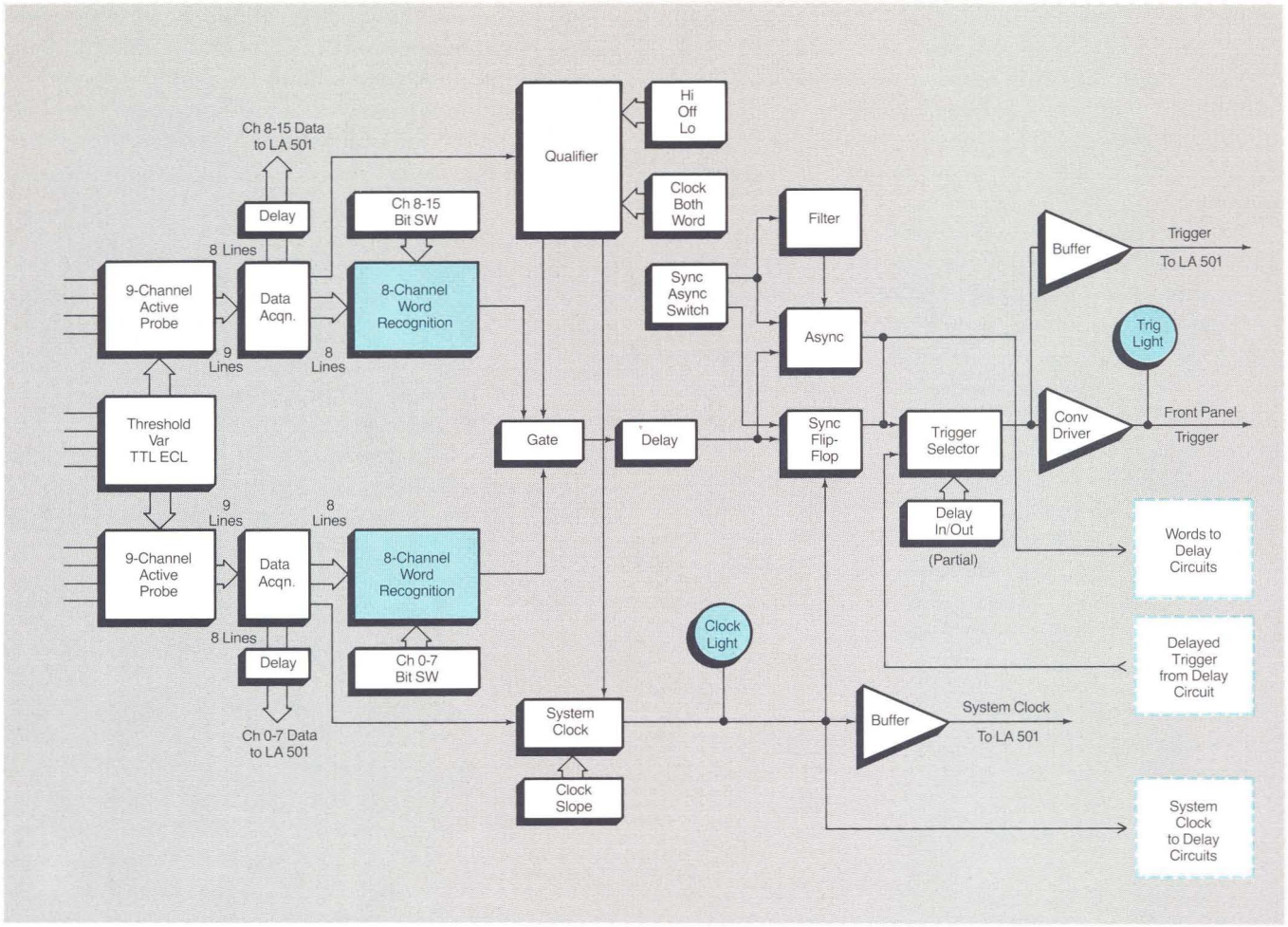


Fig. 1. Simplified block diagram of the word recognizer portion of the WR 501. Signals from the sixteen data input channels can be coupled directly to the LA 501W independent of word recognizer operation.

The 5 to 300 ns filter is activated whenever asynchronous triggering is selected, and can be set to assure valid word recognition.

Output trigger selection is controlled by the front-panel switch labelled CLOCK-OFF-WORDS, which corresponds to the Delay In/Out blocks in the diagrams. In the delay OFF position, the word recognizer output goes directly to the output buffer and output converter driver. The converter transforms the output signal from ECL to TTL level.

In the delay IN position, which corresponds to either delay by word or delay by clock, the delay circuitry is inserted in the trigger output path and no trigger output signal is generated until after the selected delay has been accomplished.

Moving along to the delay circuitry block diagram shown in figure 2, we see that the Delay By Selector routes either the system clock or the output from the word recognizer to the counter circuitry. The word recognizer output also goes to the start circuitry to initiate counting.

Five decade counters are used. The least-significant-bit (LSB) counter is ECL, with the remaining counters TTL. Counter operation is essentially straight-forward, using a 9's complement scheme. The Hold block is a latch that holds the 9999 Detector output level until the LSB counter reaches the nine count, while allowing the TTL counters to be reset.

When the selected count is reached, the Delay Output Flip-Flop is switched, generating a delayed trigger signal. The delayed trigger is routed to the Trigger Selector for availability as the output trigger signal.

Summary

The TM 500 Series family is designed to allow you to configure your measurement package to fit your measurement needs. The high-performance LA 501 has been meeting many of your logic analyzer needs. Now, the WR 501 with its high-impedance probes, 17-bit word recognition, and digital delay expands your logic analysis capabilities to include even the more sophisticated measurements. And you are not limited to the en-

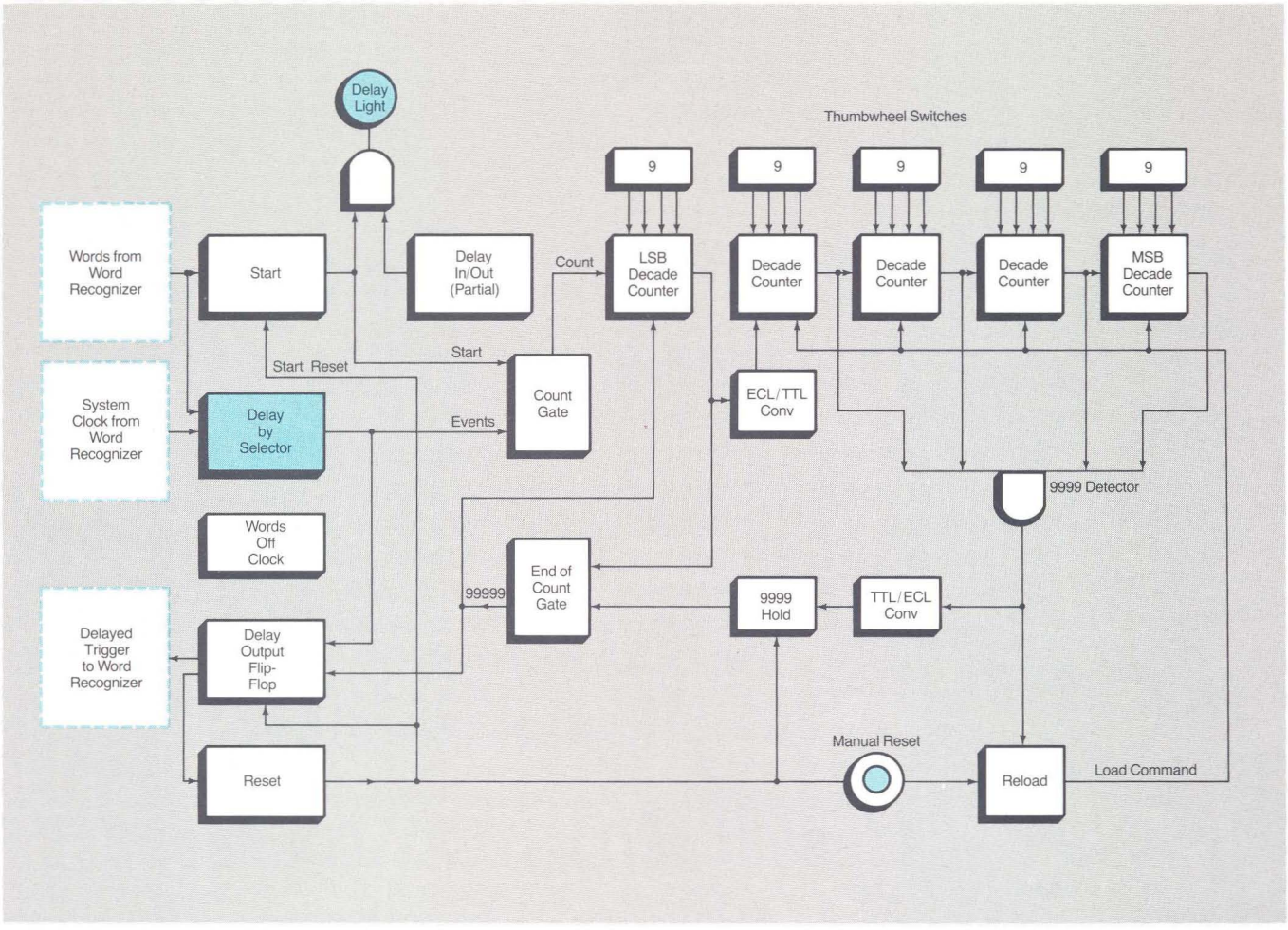
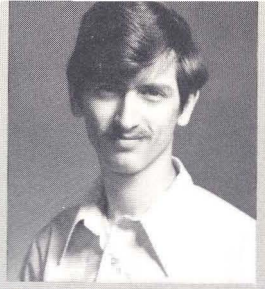


Fig. 2. Simplified block diagram of the digital delay portion of the WR 501. Delay is enabled by the word recognizer output. Manual reset provides for resetting the counter whenever the full count has not been reached.

gineering and production environment. The LA 501W, WR 501, and the SC 502 packed into a TM 515 mainframe give you a complete logic analysis system in a suitcase. They will help you solve those tough logic problems, wherever you encounter them.

Acknowledgments

Overall planning for the WR 501 was coordinated by Rod Bristol, Program Manager, with Pete Janowitz, Project Manager, responsible for translating the plans into physical reality. Milt Klaudt and Dennis Glasby performed electrical design, with Mike Lancaster fitting all of the pieces together in a very functional package. Jaime Navia contributed valuable inputs to mechanical design. Prototype support was provided by Helen Steinmetz; electrical and mechanical evaluation by Carl Matson and Merle Nielsen. Yvonne Hallock did the instruction manual. Our thanks to these and the many others who assisted in the WR 501 project.



Ira Pollock

The FG 504--a new standard in function generators

At 40 MHz, with 6-ns rise time, Tek's new FG 504 is the fastest function generator available today.

But what should really get function-generator users excited is that the FG 504 combines more features than any other generator on the market. Most of the operating modes are independent. And the front-panel controls allow *simultaneous* usage. Yet it is no more complicated to operate than your average function generator.

What all of this refinement and versatility will mean to many users is an opportunity to make one instrument do the job of several, to a degree never before possible. For example, many users will not have to buy a separate pulse generator.

A few specs. The TEKTRONIX FG 504 is a two-module-wide, 40-MHz, 6-ns rise time function generator with 30-V p-p output, variable rise and fall, log and linear sweep, phase lock, and amplitude modulation capability. Its calibrated frequency range is 0.001 Hz to 40 MHz in ten decades, with an extra range from 20 Hz to 20 KHz for audio applications. The audio range can be changed to an intermediate or custom range by replacing an internal capacitor.

A clean sweep

Using this one instrument, customers can sweep test audio amplifiers, speakers, tone controls, filters, and graphic equalizers. With sweep widths to 1,000:1, the FG 504 can sweep the entire 20-Hz to 20-KHz audio band.

The audio band, of course, is not the only frequency range the FG 504 will sweep: mechanical resonances at low frequencies and slow sweep rates are as easy to investigate as the center frequency of an IF filter. Both internal logarithmic and linear sweeps allow the user to sweep up to the 1,000:1 frequency range as fast as 100 μs, or as slow as 100 seconds. Setting the lower and upper limits is quickly accomplished with concentric START and STOP dials.

Now here's convenience. If you're involved in an application that requires frequent switching between two frequencies — such as checking filter or amplifier bandwidths — you simply pre-set your upper and lower frequencies. Hit TRIG SWEEP and you get the lower frequency. Hit the STOP FREQ button and you get the upper frequency.

The internal sweep can be manually or externally triggered, with settings ranging from +1 V to +10 V. A linear sweep output voltage (0 to +10 V) simplifies log frequency plots when sweeping the main generator logarithmically. Semi-log paper can then be used on a chart recorder.

A welcome feature is the HOLD button that allows you to "freeze", or stop, the output voltage at all frequencies below 400 Hz. People using sub-audio frequencies are often involved with analog simulations or electromechanical experiments, such as mechanical stress analysis or servo-system testing. If, in the course of an experiment, it is desirable to stop the progress and examine some intermediate result, the FG 504 allows the user to do so, retaining the voltage. This simplifies testing where you want to stop and measure a slowly changing voltage, or stop a system that you're controlling with the FG 504's output. Releasing the button lets the generator resume operation from the point of interruption.

External modulation capabilities

External control of frequency over the 1,000:1 frequency range is available via the voltage-controlled frequency (VCF) input. Signals applied to this input cause frequency modulation. The carrier frequency can be as high as 40 MHz, with a modulation bandwidth of dc to 16 KHz at maximum frequency deviation (higher with less than 1,000:1 deviation).

Digital data is often transmitted using Frequency Shift Keying (FSK). FSK can be generated by applying the digital pulse train to the VCF input and manipulating the "1" level, and setting the carrier frequency to the appropriate "0" frequency.

Automatic AM

Complementing the FM capabilities is a dc-coupled AM input that provides either external voltage control of the sine wave amplitude or standard AM.

On the FG 504, AM is automatic. Just plug the signal into the AM input and the carrier amplitude is cut in half. A positive-going signal increases the amplitude, and a negative-going signal decreases the amplitude to full, 100% modulation.

With a dc offset on the modulating signal, double-sideband, suppressed-carrier modulation is possible. Modulation bandwidth is dc to >100 KHz.

Dynamic reaction of AGC, squelch, or other amplitude-sensitive circuits, such as Dolby systems, are easy to test with a square wave on the AM input, which varies the output between two different signal levels.

For classroom use, the FG 504 can be used to demonstrate modulation theory. Modulation ability is also of great interest in the fields of receiver design, testing, service, and analysis.

Phase lock — a new feature

Until now, phase lock has been largely ignored by designers of function generators. This is rather surprising when one considers how much the ability to lock the frequency and phase of a signal generator to that of a reference signal increases the versatility of the generator.

Applications for a phase-locked function generator abound in both the analog and digital world. The design of push-pull amplifiers, for example, is greatly facilitated with signal generators that can produce both sine and square waves that are 180° out of phase.

Measuring the square-wave response is a convenient method for deriving frequency-response information: risetime—upper 3-dB frequency; sag—lower 3-dB point; overshoot—damping and pass-band flatness. This is an ideal application for a phase-locked FG 504 and another function generator such as the FG 503. The same setup can be used to analyze quadrature-phase detectors by changing the phase difference to 90°.

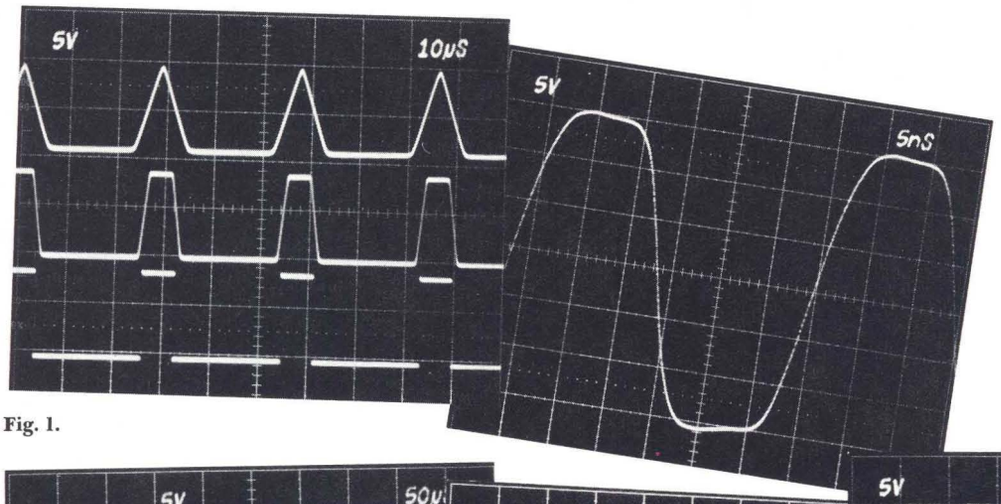


Fig. 1.

Fig. 2.

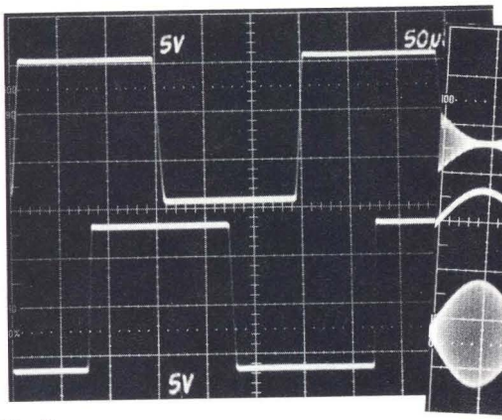


Fig. 3.

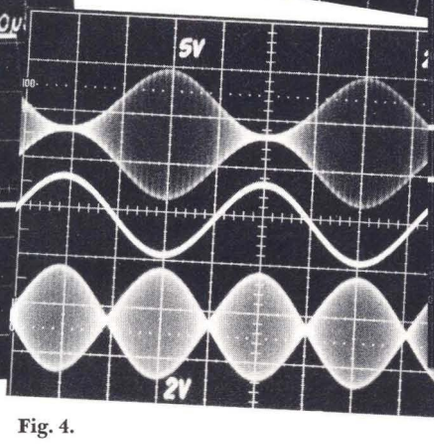


Fig. 4.

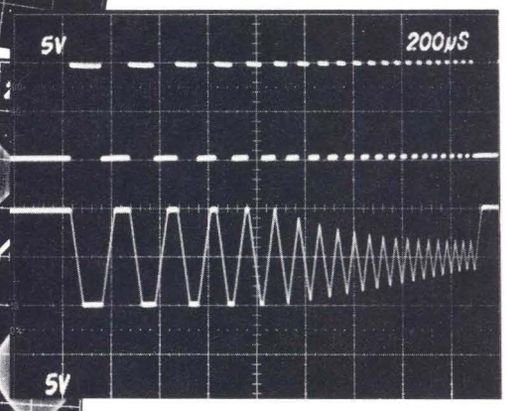


Fig. 5.

Fig. 1. Variable rise and fall times increase pulse flexibility as shown in this photo.

Fig. 2. The FG 504 provides 30 V output with 6 ns rise and fall times, ideal for design in MOS and other logic families.

Fig. 3. Generating multi-phase clock signals is greatly facilitated by the phase-lock capability in the FG 504. Slaved to a master generator, the FG 504 will follow over a wide rep rate range.

Fig. 4. A true four-quadrant multiplier permits normal AM or double-sideband, suppressed-carrier modulation.

Fig. 5. The upper trace is a frequency-swept square wave signal to an op amp. The lower trace is the op amp output, showing slew-rate limitation.

The obvious application for phase lock is to lock an FG 504 to a house standard or crystal oscillator, and have an extremely stable source of high-amplitude sine, square, and triangle waves. Adding a DD 501 to the FG 504 permits integer-frequency division, for limited synthesizer applications. For example, a 20-MHz reference divided by 247 yields a 12.35-μs period, within 0.05% of the time for a radar mile.

With a digital logic signal for a reference, and the variable phase used to set relative timing, the FG 504 output can be adjusted to give a bi-phase clock. A bi-phase clock can help to solve logic-race problems. Most microprocessors use bi-phase clocks. Using a phase-locked function generator, instead of a pulse generator with delay, has the advantage that changes in the master-generator frequency will not perturb phase relationships.

The FG 504 can be phase-locked from 100 Hz to 40 MHz. Lock and capture range is $\pm$ 10 major dial divisions ($\pm$ 10X frequency multiplier setting). With the dial set at 11, for example, the lock range is from 1 on the dial to 21.

Gated and triggered modes

Another feature that adds to the versatility of the FG 504 is the gated mode. An external signal or the manual push button can control the number of cycles that are generated in a burst, as well as the time that the burst is initiated. The use of a DD 501 with the FG 504 makes counted-burst operation possible where the user selects thumbwheel switches in the DD 501 to determine the number of cycles to be generated in the burst.

In addition to use with digital logic, gated operation is used in such acoustic applications as tone-burst testing of loud speakers, sonar, ultrasonic imaging, and anomaly detection. The starting phase of the output waveform is adjustable over a $\pm$ 80° range.

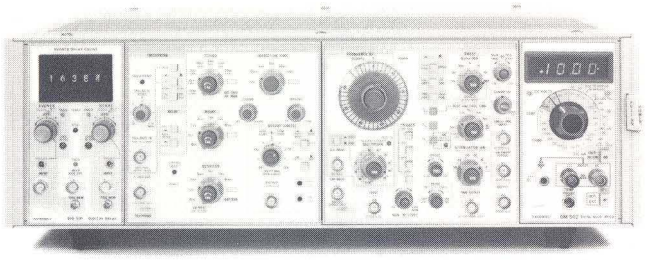


Fig. 6. Typical logic package consisting of a TM 506 Mainframe, DD 501 Digital Delay, PG 508 Pulse Generator, FG 504 Function Generator, and DM 502 Digital Multimeter.

In the triggered mode, the FG 504 generates a single cycle of the selected waveform for each cycle of the input signal, or every time the manual button is pushed. As in the gated mode, the starting phase of the selected waveform is variable over a ± 80° range. With square waves, the phase control acts as a delay control with a range of about 90% of the pulse duration.

Triggered operation is particularly useful in logic applications such as pulse shaping and level shifting. For example, a short-duration, ECL-amplitude pulse can be converted to a CMOS-level pulse of longer duration, or a sine wave can be turned into a TTL-level square wave.

Square waves are not the only useful type of triggered waveform. Triggered triangles and sine waves are used in mechanical-impulse tests. With the phase control at one end, sine-squared pulses are approximated. Sine-squared pulses find wide application in such areas as transmission-line testing, or testing the impulse response of bandwidth-limited systems, since the energy in a sine-squared pulse is concentrated in a narrow band.

The Dirac Delta function, in comparison, ideally requires infinite bandpass, and so rules itself out of these applications.

A unique output amplifier

The output section of the FG 504 is unique for a function generator. As in most function generators, the output amplifier acts as a voltage source behind 50 ohms. *Unlike* most other function generators, the signal swing at the output amplifier is a constant 30 V peak-to-peak.

Past generators have placed the variable control in front of the output amplifier and also summed the offset terminal at the amplifier input. This is an excellent scheme, due to its simplicity and low cost, for a low-performance generator.

However, in high-performance instruments problems arise. Fast output amplifiers tend to change rise time and aberrations with signal amplitude and offset. These problems are avoided in the FG 504 by running a constant-amplitude signal into the amplifier and doing all of the attenuation and offsetting after the amplifier.

The signal can be attenuated up to 50 dB, in 10 dB steps, by a step attenuator, and a constant-impedance variable attenuator can add another 20 dB.

A post-attenuator offset

Probably more important to the user than the post-amplifier attenuators is the post-attenuator offset. Dc offset is generated with an adjustable current source wired in parallel with the amplifier and attenuators. Offset range is ± 7.5 V, independent of signal level.

Users will find this arrangement particularly convenient in determining optimum bias points for amplifiers, logic thresholds, and comparator hysteresis limits.

The 50-ohm output impedance has a low-reactive component, providing minimum aberrations to signals delivered to reactive loads or at the end of unterminated cables. This allows the user to take advanage of the full 30-V signal swing, even with 6-ns rise time pulses, to drive MOS circuitry or to observe the large-signal transient response of linear circuits.

Not all pulse generator applications call for fast-rise pulses. The variable rise- and fall-time feature of the FG 504 facilitates testing of circuit parameters such as amplifier slew rate or comparator response time.

Most of the logic families now in use have a linear region in the middle of their swing. Observation of the effects of traversing this region is made easier with longer transition times on the input signal. In the FG 504, the rise and fall times of the square wave are adjustable from 10 ns to 100 ms.

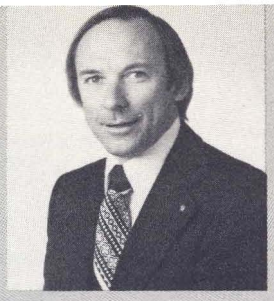
Finally — independence means versatility

A major way of insuring the versatility of the FG 504 was to make the features as independent as possible. For example, the sweep operates independent of the other sections, so it can be used to trigger or gate the function generator.

By taking advantage of the 1-V to 10-V trigger level on the input and using the triggered sweep with the FG 504 in the triggered mode, the user has a simple delay generator. Delay times from 10 μs to 100 s are possible.

Using the free-running sweep as the gating signal, the user can have a free-running burst generator with either single-frequency bursts (sweep width set to zero) or swept bursts. An external signal can be used to trigger swept bursts.

The FG 504 is currently available as a stand-alone unit, complete with mainframe and power supply; or as part of a measurement system comprising other TM 500 modular instruments.



Ron Lang

A new low-cost 500 MHz probe

Many of us take for granted that an oscilloscope display is an accurate representation of a circuit waveform. This is not necessarily true. An oscilloscope has an input impedance of typically 1 MΩ paralleled by 15 to 20 pF. A probe of some sort usually is used to extend the input of the scope to the circuit under test. There is also a certain resistance and capacitance associated with the probe. When the probe is connected to the oscilloscope, an overall impedance of the probe/oscilloscope system is presented to the circuit being measured. This loading of the circuit under test can appreciably alter the signal to be measured, as evidenced by the photo in figure 1.

There are three main characteristics of a probe that determine its ability to couple the signal to the oscilloscope without altering it: input resistance, input capacitance, and bandwidth. The input resistance should be high enough to prevent changing the signal amplitude; input capacitance should be low enough to have negligible effect on signal rise time; and bandwidth should be wide enough to faithfully reproduce the signal waveshape.

An active probe is best-suited to meet all of these requirements. For example, the new P6202 FET probe has an input impedance of 10 MΩ and 2 pF, and a bandwidth of dc to 500 MHz. Let's compare this with the typical passive probe having an input impedance of 9 MΩ and 12 pF, and a bandwidth of 250 MHz or less, and see how each affects the signal under test.

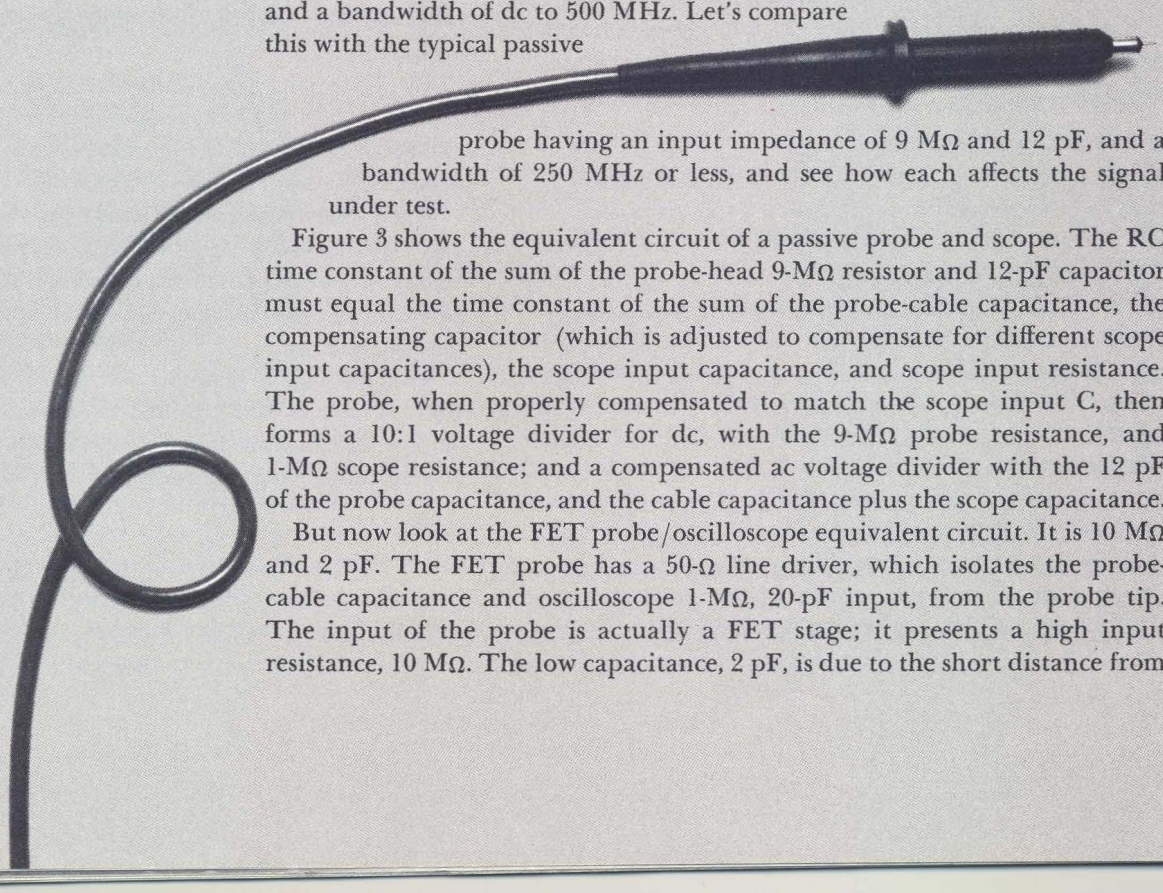


Figure 3 shows the equivalent circuit of a passive probe and scope. The RC time constant of the sum of the probe-head 9-MΩ resistor and 12-pF capacitor must equal the time constant of the sum of the probe-cable capacitance, the compensating capacitor (which is adjusted to compensate for different scope input capacitances), the scope input capacitance, and scope input resistance. The probe, when properly compensated to match the scope input C, then forms a 10:1 voltage divider for dc, with the 9-MΩ probe resistance, and 1-MΩ scope resistance; and a compensated ac voltage divider with the 12 pF of the probe capacitance, and the cable capacitance plus the scope capacitance.

But now look at the FET probe/oscilloscope equivalent circuit. It is 10 MΩ and 2 pF. The FET probe has a 50-Ω line driver, which isolates the probe-cable capacitance and oscilloscope 1-MΩ, 20-pF input, from the probe tip. The input of the probe is actually a FET stage; it presents a high input resistance, 10 MΩ. The low capacitance, 2 pF, is due to the short distance from

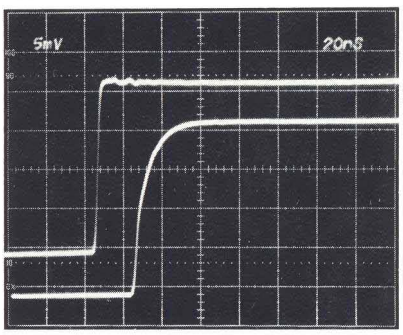


Fig. 1. The lower waveform shows the rise time of a circuit as measured using a passive probe with 10 pF input capacitance. The upper waveform shows the result using an active FET probe with less than 2 pF input capacitance.

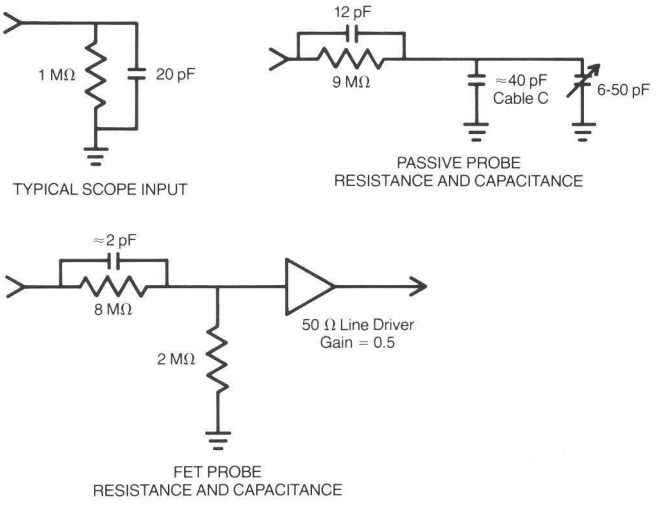


Fig. 2. Typical input resistance and capacitance of a scope, passive probe, and FET probe. Both probes provide 10 X attenuation.

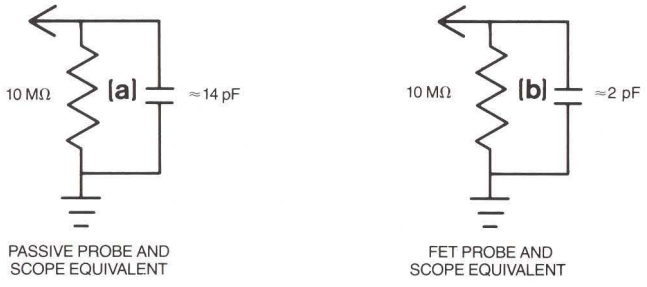


Fig. 3. Equivalent input resistance and capacitance of (a) passive probe and scope, and (b) FET probe and scope.

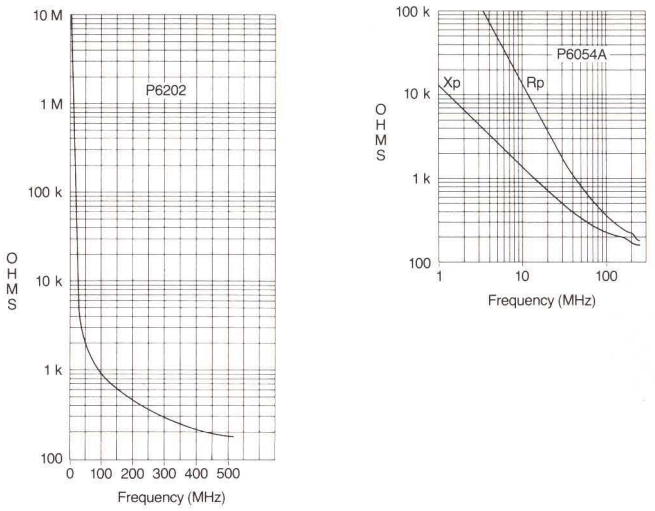


Fig. 4. Input impedance versus frequency for a P6054A passive probe, and an active FET probe. R_p of the FET probe remains essentially constant throughout its bandpass.

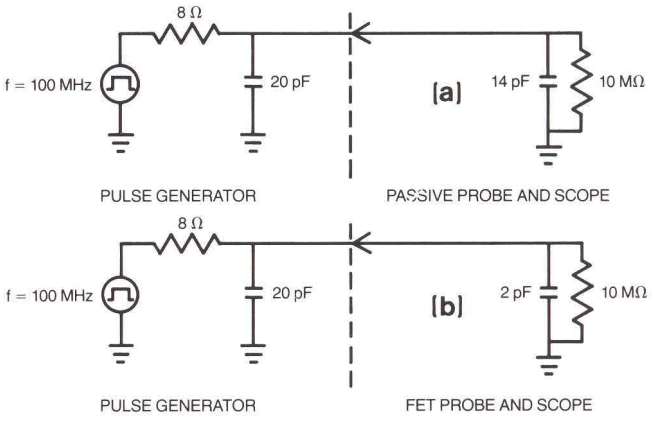


Fig. 5. Equivalent of (a) passive probe and scope, and (b) FET probe and scope applied to a fast-rise pulse generator.

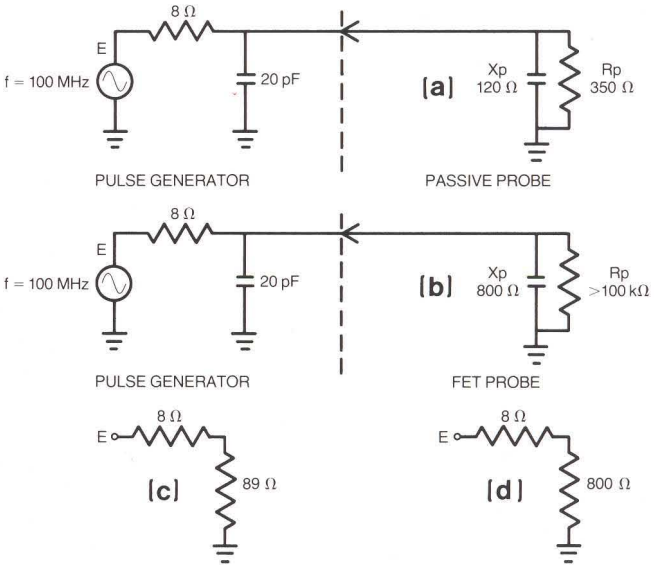


Fig. 6. Change in output amplitude of 100-MHz signal is greater with passive probe than with FET probe due to reactive elements in probe. Equivalent circuit (c) is with passive probe, and (d) is with FET probe.

the probe tip to the FET, plus the low input capacitance of the FET. The FET drives a 50-Ω line-driver stage that drives the cable from the probe head to the compensation box. The compensation box contains the output amplifiers, dc offset controls, and a switch to "switch out" the 50 Ω load if the scope input is 50 Ω instead of a high impedance.

Figure 4 shows the effects of input resistance, R_p, and input capacitance, X_p, versus frequency, for a passive probe and a FET probe. The passive probe R_p falls to about 350 Ω at 100 MHz; X_p is about 120 Ω at 100 MHz. The R_p of the FET probe remains fairly constant throughout the frequency range and is high enough in resistance to not enter into the circuit-loading calculations. The X_p is 800 Ω at 100 MHz.

Assuming a circuit source impedance of 8 Ω and 20 pF, consider rise time and amplitude effects of a passive probe and a FET probe on the circuit. See figure 5. In a pulse circuit, the t_r of the circuit is:

$$t_r \text{ circuit} = 2.2\,RC = 2.2 \times 8 \times 20\text{ pF} = 0.35\text{ ns}$$

Assume t_r of pulse is 0

With the passive probe attached, the t_{rpp} is:

$$t_{rpp} = 2.2 \times 8 \times 34\text{ pF} = 0.6\text{ ns}$$

t_{rpp} = t_r of circuit with passive probe

With the FET probe attached, the t_{rFET} is:

$$t_{rFET} = 2.2 \times 8 \times 22\text{ pF} = 0.39\text{ ns}$$

t_{rFET} = t_r of circuit with FET probe

$$\frac{t_{rpp} - t_r \text{ circuit}}{t_r \text{ circuit}} \times 100 = \frac{0.6\text{ ns} - 0.35\text{ ns}}{0.35\text{ ns}} \times 100 = 71\%$$

$$\frac{t_{rFET} - t_r \text{ circuit}}{t_r \text{ circuit}} \times 100 = \frac{0.39\text{ ns} - 0.35\text{ ns}}{0.35\text{ ns}} \times 100 = 11\%$$

With the passive probe there is a 71% change in rise time due to the input C of 14 pF, but only an 11% change with the FET probe due to the lower input C of 2 pF.

Now consider the amplitude effects with the passive and active probes. When the passive probe is attached to the circuit (see figure 6 (a)), it presents an impedance of the R_p and X_p at 100 MHz. Ignoring the phase angle because it is small, the equivalent circuit looks like figure 6 (c). The waveform presented to the scope is then, $\frac{E \times 89}{89 + 8} = 0.92E$, an 8% change.

Now consider the FET probe attached to the same circuit (see figure 6 (b)). The X_p is equal to 800 Ω at 100 MHz. The equivalent circuit with the probe attached is as figure 6 (d), $\frac{E \times 800}{808} = 0.99E$, a 1% change.

The higher input impedance of the FET probe has a smaller effect on t_r and amplitude.

FET probe advantages

The first advantage of a FET probe, then, is very low input capacitance and very high input resistance, resulting in less circuit loading and truer signal representation.

The FET probe has an active input that provides low input capacitance and a higher frequency response than a passive probe. The frequency response of the P6202 FET probe is dc to 500 MHz (-3dB).

The P6202 also has dc offset capabilities. This means that any dc voltage up to ±55 volts can be offset without any degrading of the probe response. The advantage is to measure a small ac voltage on a large dc component, at the full bandpass capabilities of the probe. A switch on the compensation box allows the dc offset to be switched in or out.

Another switch on the output connector of the compensation box allows the probe to be used with either 50-Ω or high-impedance inputs. When used with a 50-Ω input, the 50-Ω load in the output of the probe is switched out. When using high-impedance inputs, the 50-Ω load is switched in.

A built-in power supply allows the P6202 to be used on any instrumentation, including counters, without having an external power supply or accessory power available. It can be used with 115 or 230 VAC, 50 to 60 Hz power sources.

Optional accessories are a slip-on ac coupling cap to block unwanted dc components (above the 55 volts of dc offset), and a slip-on 10X attenuator to make the input 100 times attenuation, still at 10-MΩ and 2-pF input impedance.

Summary

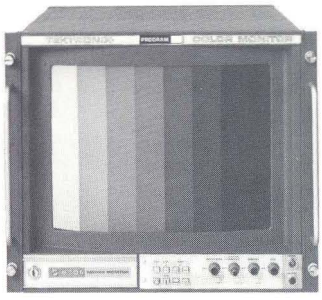
The new low-cost P6202 FET probe offers several advantages over the passive probe for many applications: wide bandwidth, very low input capacitance, high input resistance, dc offset, usable with either 50 Ω or high impedance inputs.

Small and rugged, the P6202 can get into tight places and yet stand the rigors of production and testing.

The 0 to ±6 volt dynamic range and ±55 volt offset capability make this low-cost probe applicable to a diversity of measurement needs. The optional 10X attenuator and ac coupling heads extend the operating range of the P6202 still further.

The P6202 includes a BNC connector that provides scale readout on the 10X mode to instruments having readout capability, yet maintains compatibility with non-readout instruments.

New Products
New Products
New Products



670A Picture Monitors

The new 670A Series consists of precision color picture monitors for NTSC and PAL Television standards. The series uses a 17-inch Triniton to present a picture whose sharpness is enhanced by a new feature – variable aperture control. The monitors are factory set for an accurate white balance at D6500°, however, you may choose to adjust to your own standards.

Consistency between TEKTRONIX Monitors is a major benefit. In the 670A Series consistency is achieved through use of the simple-to-converge Trinitron, excellent clamp stability, and a highly regulated EHT. Less than 1% change in raster size will occur with large APL changes, and blanking and black level are extremely stable, too.

Individual lines in the vertical interval can be examined in detail using the expanded vertical delay mode. Horizontal delay is also provided. The 670A features inputs isolated from ground, eliminating the need for special hum-bucking transformers. Optional outputs are available that take advantage of the precision decoding circuits of this monitor series, to provide an accurate vectorscope display using a low-cost x-y monitor. The monitors are compact, requiring only 15.75 inches of rack space.

1405 Television Sideband Adapter

The 1405 Television Sideband Adapter is used with a spectrum analyzer, such as the 7L12 or 7L13, to analyze the sideband response of a television transmitter.

Connected to the 7L12 or 7L13, the 1405 generates a composite-video signal, the picture portion of which is a constant-amplitude sine wave signal that sweeps from 15-0-15 MHz. When this signal is used to modulate the TV transmitter, the sideband response of the transmitter will be displayed on the spectrum analyzer.

The 1405/Spectrum Analyzer combination can be used to display the frequency-response characteristics of RF and IF stages of any VHF or UHF transmitter used today in the world. Six crystal marker positions are provided.

In addition to sideband testing, typically done in a TV station once a week, the 1405/Spectrum Analyzer combination can perform the following tests: log amplitude display of sideband response, in-service testing, spectrum analysis of the transmitter, differential gain measurements, aural transmitter deviation, antenna VSWR (with directional coupler), baseband response, and complete loop testing including STL.

1410 Series NTSC Generators

The new 1410 Series of NTSC Sync Pulse and Test Signal Generators are high-performance instruments offering all the advantages of modularity, at prices generally associated with units of single-piece construction. To suit your specific needs, you may choose from a wide selection of sync-pulse and test-signal generator functions to be combined with the mainframe providing the color standard of your choice. Should you develop additional test-signal requirements in the future, plug-in card construction insures a quick and easy retrofit for you. Any combination of five test-signal generator modules driven by one sync-pulse generator is feasible.

The Sync Pulse Modules and the Test Signal Modules plug vertically onto the 1410 Mainframe interface board. Front-panel controls and switches are mounted on the module with easily-removable extenders projecting through the front panels. Available modules include three sync-pulse generators, a color-bars generator, a convergence pattern generator, a linearity signal generator, and a VIRS/Black Burst generator.

1470 and 1474 CCTV Signal Generators

Two new signal generators, the 1470 and 1474, are designed specifically to economically meet the needs of CCTV operations.

The first generator, the 1470 CCTV Color Sync and Test Signal Generator is a compact, economical unit designed to provide gen-lock sync plus a selection of

high-quality full-field test signals. Among the sync and timing features of the 1470 is the ability to color gen-lock to composite video from all normal sources, including most helical scan video tape recorders. (When gen-lock operation is not required additional savings will be gained by ordering Option 1.)

The second generator, the 1474 CCTV Color Sync Generator, has the performance features of the 1470 but does not produce test signals.

Sync pulse generation

The sync pulse functions of the 1470 and 1474, like those of other TEKTRONIX generators, are of broadcast quality. These generators can operate as master sync generators or as units fully or partially timed from external sources. Color gen-lock of the highest quality is a standard feature.

Front-panel push button selection of external subcarrier and sync is provided for your convenience. If external subcarrier is lost, the 1470 and 1474 start monochrome operation automatically and a warning light appears.

Test signals

Push-button selection of test signals in the 1470 simplifies your testing operations. When you select color bars, multiburst, convergence, or window; each test-signal push button used cancels any other test signal selection. To make a linearity test with a staircase signal, you use only two buttons: Subcarrier on/off and high, low or medium APL. For flat-field testing the 1470 has the unique ability to produce red, green or blue signals to simplify color picture monitor adjustment by eliminating the need to turn beams on and off. Flat-field white is produced by depressing all three buttons. Yellow, cyan, or magenta fields are available by just depressing two of the three buttons. Each test signal is of the highest standards of the industry, providing essentially aberration-free transitions and accurate, flat levels.

AM 511 CATV Preamplifier

The AM 511 CATV Preamplifier is a TM 500 Series plug-in unit designed to operate as an accessory for the 7L12 and 7L13 Spectrum Analyzers. It is particularly useful for measuring-signal-to noise, radiation, and field intensity to FCC specifications on CATV, television, and FM installations. Other uses include radio-system servicing and measurements, as well as increasing sensitivity for EMI measurements within the 30- to 890-MHz frequency range.

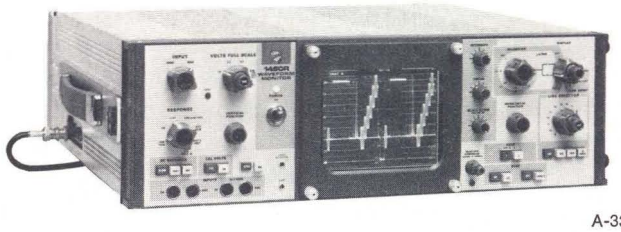
The AM 511 is also an excellent amplifier for use with any wideband scope such as the 475 or 485, or with the 7A16 or 7A19 where low-noise nanovolt sensitivity is desired.

Input impedance is 75 Ω. Reference level is calibrated in 1-dB steps from +79 dBmV to 0 dBmV. Intermodulation distortion is at least 70 dB down. VSWR is 2:1.

1480 Option 6 Waveform Monitor

The 1480R Option 6 is a high-performance television waveform monitor designed for use in your television operating center or by your field service force. Option 6 is especially designed for measurements in long-distance, video transmission systems using 124-Ω balanced lines. Self-normalizing WECO-style input jacks allow this instrument to operate in a 75-Ω system without externally terminating the ring input. With these features the 1480R Option 6 has been designed to operate in either a 124-Ω balanced or 75-Ω unbalanced system.

Vertical sensitivity, with automatic bandpass limiting, has been increased to 0.05 volts full scale for making differential phase and gain measurements with Bell Kelley or Telemet Test Sets. A 5- to 12-second, variable sweep has been added to measure low-frequency distortions and system bounce caused by large APL changes in the video signal.



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